



# DIGITAL IC DESIGN

## PROF. JANAKIRAMAN

Department of Electrical and Electronics Engineering  
IIT Madras

**PRE-REQUISITES** : A course on digital logic design is a must for doing this course.

**INTENDED AUDIENCE** : Any student interested in Circuit Design as applied to VLSI Design

**INDUSTRIES APPLICABLE TO** : All VLSI Design companies

### COURSE OUTLINE :

This is a most fundamental Digital Circuit Design course for pursuing a major in VLSI. We do not deal with any Verilog coding during this course and instead discuss transistor level circuit design concepts in great detail. Learning objectives of this course are:

- Characterize the key delay quantities of a standard cell
- Evaluate power dissipated in a circuit (dynamic and leakage)
- Design a circuit to perform a certain functionality with specified speed
- Identify the critical path of a combinational circuit
- Convert the combinational block to pipelined circuit
- Calculate the maximum (worst case) operating frequency of the designed circuit

### ABOUT INSTRUCTOR :

Prof. Janakiraman Viraraghavan is an Assistant Professor at the Department of Electrical Engineering, IIT Madras and is part of the Integrated Circuits and Systems (iCS) group. His research interests include porting machine-learning algorithms on to hardware and statistical analysis in VLSI. He also has a keen interest in Microprocessors and Programming in general.

### COURSE PLAN :

**Week 1:** The CMOS Inverter construction and Voltage Transfer Characteristics

**Week 2:** Resistance and Capacitance and transient response.

**Week 3:** Dynamic, Short Circuit and Leakage power – Stacking Effect

**Week 4:** Combinational Circuit Design and capacitance

**Week 5:** Parasitic Delay, Logical Effort and Electrical Effort

**Week 6:** Gate sizing and Buffering

**Week 7:** Asymmetric gate, Skewed gates, Ratio'ed logic

**Week 8:** Dynamic Gates and Domino logic and Static Timing Analysis

**Week 9:** Sequential circuits and feedback. Various D flip flop circuits – Static and Dynamic

**Week 10:** Setup and Hold Time measurement. Timing analysis of latch/ flop based systems

**Week 11:** Adders – Mirror adder, Carry Skip adder, Carry Select adder, Square Root adder

**Week 12:** Multipliers – Signed and Unsigned arithmetic, Carry Save Multiplier implementation